

A ONE-WEEK TRAINING IN ELECTROMAGNETIC COMPATIBILITY OF INTEGRATED CIRCUITS

DESCRIPTION OF THE COURSE TOPIC

The five-day course is focused on electromagnetic compatibility of integrated circuits.

A set of basic concepts is proposed as an introduction, covering specific units, parasitic impedance of interconnects, origin of noise, noise margins, time/frequency conversion and adaptations.

The second focus concerns parasitic emission, how to design low emission circuits and how to measure the IC emission using standard IEC 61967 methods.

A third topic concerns susceptibility, with focus on measurement methods [IEC 62132] and hardware/software techniques to improve immunity to interference.

The fourth part is related to modeling approaches for predicting EMC [IEC 62433], based on standards such as IBIS, ICEM and ICIM.

The fifth part deals with EMC guidelines for improved emission and immunity to interference. Finally, roadmaps and future challenges are briefly reviewed. Illustrations of these concepts are made using IC-EMC (www.ic-emc.org), a freeware including unique features and tools for efficient EMC simulations of integrated circuits. Afternoons are dedicated to practical sessions including an access to the EMC laboratory of INSA Toulouse, for hands-on experiments of IC emission characterization (according to IEC 61967) and IC immunity characterization [IEC 62 132].

Lecturers

Etienne Sicard

Graduated from the University of Toulouse [B.S degree in 1984] and obtained a PhD in 1987 at LAAS/ CNRS laboratory

Alexandre Boyer

Graduated from INSA engineering school in 2004 and obtained a PhD in 2007 in electromagnetic compatibility of Integrated Circuits

INEOS

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Durée du stage :
5 jours - 30 heures

 Price: 2050€ per person; 1600€ for IEEE or SEE members; 990 € for PhD Master Students.

lunches included

Renseignements & inscription :

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